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Description

Vertical Carbon Nanotube Field Effect Transistor

BACKGROUND OF INVENTION

[0001] TECHNICAL FIELD

[0002] The field of the invention is that of integrated circuit fabrication, in particular forming field effect transistors (FETs) using carbon nanotubes to provide the body of the FET.

[0003] It has been established that carbon nanotubes with the proper molecular structure may act as semiconductors.

[0004] Some attempts have been made to fabricate FETs using a carbon nanotube as the body of the transistor.

[0005] There have been problems in such attempts with producing FETs with well controlled channel lengths. As those skilled in the art are aware, variation in channel length affects the capacitance of the transistors and thus the timing of the transistor action.

[0006] Also, due to the difficulty of manipulating carbon nanotubes and due to the difficulty of controlling the growth

of carbon nanotubes parallel to a wafer/substrate surface, the gate is usually the silicon wafer/substrate and the insulator is an oxide grown on the surface of the silicon wafer.

[0007] The results of such attempts, though they demonstrate that carbon nanotubes may be used as the transistor body, produce primarily experimental devices, not suited to mass production.

[0008] A potential benefit of FETs based on nanotubes is that they have very small diameters, approximately 5 - 50nm and thus can theoretically be very closely packed.

[0009] Close packing has the very great potential benefit of increasing the density of devices - a highly desirable result.

SUMMARY OF INVENTION

[0010] The invention relates to a FET having a vertical carbon nanotube as the transistor body.

[0011] A feature of the invention is the use of a layer of deposited conductive material as the transistor gate, thereby establishing close control over the channel length that does not depend on lithography.

[0012] Another feature of the invention is the formation of an aperture within the gate layer, followed by deposition of a gate insulator on the walls of the aperture, and deposition

of a nanotube within the aperture.

[0013] Another feature of the invention is the use of a lateral conductive layer as the transistor source and drain.

Brief Description of Drawings

[0014] Figure 1 shows a section of an integrated circuit containing a completed carbon-nanotube FET according to the invention.

[0015] Figure 2 shows the same area at a preliminary step, before patterning the deposited layers.

[0016] Figure 3 shows the same area after processing to expose steps for the formation of a source contact.

[0017] Figure 4 shows the area after etching a via through the gate conductor layer.

[0018] Figure 5 shows the area after deposition of a catalytic layer to promote the formation of the desired molecular structure within the nanotube.

[0019] Figure 6 shows the area after forming the gate insulator.

[0020] Figure 7 shows the area after formation of the carbon nanotube within the aperture.

[0021] Figure 8 shows the area after deposition of insulating layers enclosing the FET structure.

[0022] Figure 9 shows the area after formation of contacts to the

transistor source, drain and gate.

Detailed Description

[0023] Figure 1 shows a completed vertical carbon-nanotube FET 100 according to the invention. The whole structure rests on substrate 10, illustratively a silicon wafer conventionally used for integrated circuit fabrication. Silicon will not be required in general, unless other portions of the circuit use silicon transistors or other structures that make use of the well known properties of silicon.

[0024] Advantageously, silicon wafers are readily available and are provided with a very high degree of planarity. Other substrate materials, such as glass, may also be used if preferred.

[0025] An optional insulator layer 20, illustratively silicon oxide (SiO_2), serves to provide isolation between the transistor being formed and other areas of the wafer. If the substrate is insulating, layer 20 would not be required.

[0026] Conductor 30, illustratively doped polycrystalline silicon, is used to provide a contact and one electrode of the transistor. This layer and other layers in the structure illustrated are shown as extending across the Figure, for convenience is forming the illustration. A commercial embodiment would have the various horizontal layers patterned

to save space and increase the density of devices in the circuit.

[0027] Layer 50, illustratively an insulator such as oxide or nitride (Si_3N_4), provides isolation between source 30 and gate 60 at the center of the Figure. As will be discussed below, gate 60 and the underlying layers are provided with a high degree of planarity, so that the thickness of layer 60 is highly uniform across the circuit. The uniformity in thickness translates to a corresponding uniformity in channel length in the devices.

[0028] On the left of the Figure, a carbon nanotube 110 extends vertically, separated from gate layer 60 by gate insulator 65.

[0029] Above layer 60, insulating layer 70 is the counterpart to layer 50, separating the gate electrode from the drain electrode.

[0030] Drain electrode 82 makes electrical contact with the top portion of tube 110 above gate 60, which is the drain of the FET.

[0031] For convenience in illustration, the three contacts to the source, drain and gate have been shown as passing through the same plane. In actual devices, they will be placed, as a result of various design choices, to maximize

the packing density and minimize the capacitance between the source or drain and the gate, for example. Thus, the device designer may choose to have the various electrodes extend to the left in the figure or in or out of the plane of the paper.

[0032] Figure 2 shows a starting structure for the practice of the invention, in which a silicon substrate 10 has been provided with a layer of insulator 20, illustratively silicon oxide (SiO_2), a conductive layer 30 that will be the source of the transistor, illustratively doped polycrystalline silicon (poly), a second, relatively thin layer of insulator 50, illustratively another layer of oxide or nitride (Si_3N_4), a gate conductor layer 60, illustratively poly, and a second layer of insulator 70.

[0033] Preferably, each layer of the structure has been planarized, e. g. by chemical-mechanical polishing, at least up to the top of layer 60. As will be discussed below, the channel length of the transistors will be set by the thickness of gate conductor layer 60, so that variations in the thickness of that layer will produce corresponding variations in channel length. Variations in the thickness of the underlying layers will also produce variations in channel length.

[0034] The Figures are partially pictorial and partially schematic in nature. The thicknesses shown in the figures are chosen for convenience in illustration and do not necessarily reflect the actual relative dimensions of the various layers.

[0035] Preferably, the layers 50 and 70 are relatively thin, consistent with providing an adequate degree of insulation, as they separate the transistor channel from the source and drain electrodes and serve to limit the current provided by the transistor.

[0036] Figure 3 shows the next step in the process, in which standard lithographic and etch techniques have been used to form two steps that will be used for contacts to the electrodes. On the right, a location for the source contact is denoted with numeral 31. Above and to the left, a corresponding location 61 has been formed for the gate contact.

[0037] Figure 4 shows the preparation of the location of the carbon nanotube. A via 64 has been formed through insulator 70, gate electrode 60 and insulator 50, penetrating layer 30 enough to establish a good contact and also such that the following catalytic material to be deposited next has a top surface that is below the bottom surface of insulator layer 50.

[0038] Figure 5 shows the optional deposition of a catalyst 34, that has been found to initiate the growth of a carbon nanotube of the correct molecular structure. If the material of source layer 30 is suitable for the growth of a carbon nanotube, the catalyst may be omitted. In the case of establishing a semiconductor material, suitable catalytic materials are Ni, Co, Fe or silicides of these metals. Illustratively, the material is deposited by a CVD or PVD process. A wet etch or an isotropic dry etch is then used to clean off the catalytic material from the inner surface of layer 50, in order to assure that a residual amount of the catalyst does not short the source electrode to the gate. If the catalyst is a good insulator, this last step may be omitted.

[0039] Figure 6 shows the result of forming a gate insulating layer 65 on the interior surface of aperture 64. When the gate layer 60 is poly, it is convenient to oxidize thermally the interior surface of aperture 64 to form gate insulator 65. If the catalyst cannot stand the oxidation temperature, it may be deposited later after oxidation and a directional reactive ion etch (RIE) to form a clean surface at the bottom of aperture 64. Those skilled in the art will be aware of other alternatives, such as a nitride gate insulator or

another insulating material that may be deposited within the aperture at a lower temperature, in the event that the gate conductor material does not form a suitable oxide or if the oxidation temperature is too high for the catalyst.

[0040] An advantage of a deposited gate insulator is that it will extend continuously up past the top surface of the gate and into the interior of insulator layer 70, thus preventing any shorts between the gate and the carbon.

[0041] Figure 7 shows the structure after formation of the carbon nanotube 110, shown as extending slightly up above the top of insulator 70. Illustratively, the carbon nanotube is formed by reacting $C_2H_2 + N_2$.

[0042] Figure 8 shows the structure after deposition of a nitride barrier layer 75 and a BPSG interlevel dielectric 120.

[0043] Referring back to Figure 1, there is shown the result of forming vias to the source, gate and carbon and filling the vias with the conductive interconnect used for the circuit, e. g. copper.

[0044] Brackets 132 and 134 in Figure 1 indicate locations of additional nanotubes connected in parallel between the same source and drain and controlled by the same gate. Those skilled in the art will be aware that transistors having discrete amounts of current capacity may be formed

by connecting two or more nanotubes in parallel, depending on the load being driven.

[0045] Conventional back end processes form other interconnection layers as required to complete the circuit.

[0046] Those skilled in the art will appreciate that current technology permits the gate layer to be formed with a thickness in the range of 5 - 200nm and a tolerance of about 2% - 5%, three sigma. This provides a more uniform transistor channel length across a circuit than is practical with lithographic techniques.

[0047] The thickness of insulating layers 50 and 70 are preferably less than 5 - 50nm in order to reduce the effect of having a length of higher-resistance material in series with the transistor electrodes.

[0048] The diameter of the aperture 64 is preferably about 5 - 70nm and the thickness of the walls of the carbon nanotube is preferably about 2 - 50nm.

[0049] If desired, the chemical composition of the carbon nanotubes at the ends that meet the source and/or drain contacts may be varied, thus producing the same benefits as are currently realized by the LDD and halo implants used in planar FETs (e.g. suppressing short channel effects). Since the transistor body is being formed in a se-

quential process, it is convenient to alter the composition of only the source or only the drain interface regions to meet the device requirements. This is in contrast to the planar technology that requires implanting both ends of the channel.

[0050] While the invention has been described in terms of a single preferred embodiment, those skilled in the art will recognize that the invention can be practiced in various versions within the spirit and scope of the following claims.

[0051] What is claimed is: